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10/814,821	03/31/2004	Yuichi Ichikawa	9683/184	5312

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EXAMINER	
CAMPOS, YAIMA	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,821	ICHIKAWA ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated August 3, 2006. At this point claims 1-5 have been cancelled and claims 6-24 have been added. There are 19 claims pending in the application; there are 6 independent claims and 13 dependent claims, all of which are ready for examination by the examiner.

I. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. **Claims 12 and 14** rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. As per **Claims 12 and 14**, the preamble of these claims recite the limitation of "a computer data signal embodied in a carrier wave." Therefore, claims 12 and 14 are directed to non-statutory subject matter as these claims recite nothing more than a transmission media to transfer signals which are defined as physical characteristics of a form of energy, such as frequency, voltage, or the strength of a magnetic field; define energy or magnetism, per se, and as such are nonstatutory phenomena. Moreover, it does not appear that a claim reciting a signal encoded with function descriptive material falls within any of the categories of patentable subject matter set forth 35 U.S.C. 101.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 6-7, 11-15, 17 and 19-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzaki (US 2004/0078636) in view of Pawate et al. (US 5,678,021).

1. As per **claims 6 and 11-12** (New), Suzaki discloses a communication device comprising: **[a communication system to exchange and execute trial data (Column 1, paragraph 0002)]**

"operation input means for receiving a command from a user;" **[(Figure 6)]**

"cache memory means for temporarily storing data;" **[This limitation is disclosed by Suzaki as "disk cache 78 provided in RAM" (Column 3, paragraph 0038, lines 3-4)]**

"content storage means composed of nonvolatile memory; and" **[With respect to this limitation, Suzaki discloses "HDD 74" (Column 3, paragraph 0038, line 1)]**

"a processor configured to receive contents;" ;" ***(Page 9, paragraph 0048 of Applicant's specification identifies this means as "CPU 400")*** **[With respect to this limitation, Suzaki discloses that "trial software and trial data are exchanged via various communication media" (Column 1, paragraph 002) and "MPU 72" (Figure 6)]**

"said processor operable, when said contents are received, to write said contents in said cache memory means;" (***Pages 7 and 9, paragraphs 0034 and 0047 of Applicant's specification identifies this means as "CPU 400"***) **[With respect to this limitation, Suzuki discloses "MPU 72;" "A disk cache is a memory (usually a semiconductor memory) that is faster than the hard disk, that is used to hold data to enable hard disk data to be rewritten at high speed, for effecting high-speed access in cases where the same data is accessed a number of times, and for collectively writing to disk with an intentional delay" (Column 2, paragraph 0034)]** "and said processor further operable, in response to a command received via said operation input means to store said comments that have been processed or executed by said processor, to read said contents from said cache memory means, and to write said contents in said content storage means" (***Pages 7 and 9, paragraphs 0034 and 0047 of Applicant's specification identifies this means as "CPU 400"***) **[Suzaki discloses this limitation as "MPU 72;" "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)]**.

Suzaki does not disclose expressly "said processor further operable, after said contents are stored in said cache memory means, to process or execute said contents automatically, absent receipt of a command initiated by a user."

Pawate discloses the concept of "said processor further operable, after said contents are stored in said cache memory means, to process or execute said contents automatically, absent receipt of a command initiated by a user;" as **["within the smart memory, a processing core is operable to execute instructions in the form of instruction logic signal groups stored in that storage" wherein smart "DRAM" is capable of processing/executing contents absent a command initiated by a user (Column 2, lines 8-29; Column 2, line 65-Column 3, line 8; Column 4, lines 1-49; Column 7, lines 39-46)]**.

Suzaki (US 2004/0078636) and Pawate et al. (US 5,678,021) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the input and output control means for computer system storage having "a cache memory" as taught by Suzaki and use a "smart DRAM" having processing capability as taught by Pawate as the cache memory in the system taught by Suzaki.

The motivation for doing so would have been because Pawate discloses that using "Smart DRAMs" provides **["an important technical advantage of the present invention is the fact that system throughput can be increased through use of the present invention" (Column 2, lines 18-20) and "improved CPU to memory bandwidth" (Column 5, lines 19-21)]**.

Therefore, it would have been obvious to combine Suzaki (US 2004/0078636) with Pawate et al. (US 5,678,021) for the benefit of creating a communication system to obtain the invention as specified in claims 6 and 11.

2. As per **claim 7**(New) A communication device according to Claim 6, **[See rejection to claim 6 above]** wherein: "said processor is further operable to receive trial information

indicative that said contents are for trial use; and said processor, in response to receipt of said trial information, is further operable to write said contents in said cache memory means" **[as writes of trial data to a hard disk are made through a disk cache (Pages 2-3, Paragraphs 0034-0038)]**.

3. As per **claims 13-14** (New) A communication device comprising: **[a communication system to exchange and execute trial data (Column 1, paragraph 0002)]**

"operation input means, for receiving a command from a user;" **[Figure 6]**

"content storage means for storing contents;" **[With respect to this limitation, Suzaki discloses "HDD 74" (Column 3, paragraph 0038, line 1)]**

a processor operable to receive contents; **[With respect to this limitation, Suzaki discloses that "trial software and trial data are exchanged via various communication media" (Column 1, paragraph 002) and "MPU 72" (Figure 6)]**

"after said contents are received, said processor further operable to write said contents in said content storage means in association with a first identifier indicating that said contents are to be stored temporarily;" **[Suzaki discloses this limitation as "A disk cache is a memory (usually a semiconductor memory) that is faster than the hard disk, that is used to hold data to enable hard disk data to be rewritten at high speed, for effecting high-speed access in cases where the same data is accessed a number of times, and for collectively writing to disk with an intentional delay" (Column 2, paragraph 0034)] [Suzaki discloses this limitation as "MPU 72;" "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74**

that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)]

"and said processor responsive to a command received via said operation input means to store contents processed or executed by said processor, said processor further operable in response to said command to exchange said first identifier for a second identifier that indicates said contents are to be stored enduringly when the processor is operable to determine the content is not for trial use, the processor further operable to store the content in the second storage area, and await receipt of a command initiated by a user to process or execute the longer term stored content"

[Suzaki discloses this concept as "a software execution method" that by "using the input and output means for computer system storage, enables trial software, trial data and mail data to be safely tried" (Column 1, paragraph 0015, lines 10-14) wherein "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)].

Suzaki does not disclose expressly "said processor further operable, after said contents are stored in said cache memory means, to process or execute said contents automatically, absent receipt of a command initiated by a user."

Pawate discloses the concept of "said processor further operable, after said contents are stored in said cache memory means, to process or execute said contents automatically, absent receipt of a command initiated by a user;" as **["within the smart memory, a processing core is operable to execute instructions in the form of instruction logic signal groups stored in that storage" wherein smart "DRAM" is capable of processing/executing contents absent a command initiated by a user (Column 2, lines 8-29; Column 2, line 65-Column 3, line 8; Column 4, lines 1-49; Column 7, lines 39-46)]**.

Suzaki (US 2004/0078636) and Pawate et al. (US 5,678,021) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the input and output control means for computer system storage having "a cache memory" as taught by Suzaki and use a "smart DRAM" having processing capability as taught by Pawate as the cache memory in the system taught by Suzaki.

The motivation for doing so would have been because Pawate discloses that using "Smart DRAMs" provides **["an important technical advantage of the present invention is the fact that system throughput can be increased through use of the present invention" (Column 2, lines 18-20) and "improved CPU to memory bandwidth" (Column 5, lines 19-21)]**.

Therefore, it would have been obvious to combine Suzaki (US 2004/0078636) with Pawate et al. (US 5,678,021) for the benefit of creating a communication system to obtain the invention as specified in claims 13 and 14.

4. As per **claim 15**, the same rationale as in the rejection to claims 13-14 is herein incorporated. However, the combination of Suzaki and Pawate does not disclose that content is received from a wireless network. However, the examiner asserts that it would have been obvious to one ordinary skill in the art at the time the invention was made to use the memory as being claimed in claim 15 in a wireless. A recitation directed to the manner in which a claim is intended to be used does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987).

5. As per **claim 17** (New) the communication device of Claim 15, **[See rejection of claim 15 above]** wherein "the processor is operable to determine if the received content can be stored based on whether an indication that the content is trial content is present in the received content" **[With respect to this limitation, Suzaki discloses "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS**

kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)].

6. As per **claim 19** (New), the combination of *** discloses the communication device of Claim 15, **[See rejection to claim 15 above]** "wherein the first storage area and the second storage area are assigned areas of the memory" **[Refer to "RAM 71" and "HDD 74" (Fig. 6)]**.

7. As per **claim 20** (New) the communication device of Claim 15, wherein "the first storage area and the second storage area are identified with a respective indicator included in the data stored in the respective first and second storage areas" " **[With respect to this limitation, Suzaki discloses "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)]**.

8. As per **claim 21** (New) the communication device of Claim 15, **[See rejection to claim 15 above]** wherein "the processor is operable to automatically process or execute the temporarily stored content to enable a user to demo the temporarily stored content" **[The rationale of the rejection of claims 13-15 is herein incorporated]**.

9. As per **claim 22** (New) the communication device of Claim 21, wherein "the processor is operable to change a status of the temporarily stored content to long term stored content in response to receipt of a user command to perform such a change" **[With respect to this limitation, Suzaki discloses "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)].]**

10. As per **claim 23** (New) the communication device of Claim 22, wherein "the processor is operable to change the status by relocation of, the content from the first storage area to the second storage area" **[With respect to this limitation, Suzaki discloses "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between"**

(Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)].].

11. As per **claim 24** (New) The communication device of Claim 22, wherein "the processor is operable to change the status by modification of an indicator included in the content, wherein the indicator is modified to indicate that the content is stored longer term instead of temporarily" **[With respect to this limitation, Suzaki discloses "when writing to a first storage, writes via a disk cache of a predetermined capacity" and later performs write-back of data to "HDD 74" (Column 1, paragraph 0016 and Columns 2-3, paragraphs 00034 and 0038) wherein "when data is recorded on HDD 74 in accordance with a request from OS kernel 71 or the like, using the write-back method, data in a disk cache 78 provided in RAM is recorded via MPU 72" and explains that "a switch 73 is provided between MPU 72 and the HDD 74 that controls whether or not data flows there between" (Columns 2-3, paragraphs 0034 and 0038) wherein "the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)** .

12. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzaki (US 2004/0078636) in view of Pawate et al. (US 5,678,021) as applied to claims 6-7 above, and further in view of Wong et al. (US 2004/0111443).

13. As per **claim 8**, Suzaki discloses (New) a communication device according to Claim 6, **[See rejection to claim 6 above]** but does not disclose expressly "said processor is further operable to determine whether a size of a free space of said content storage means is equal to, or

greater than, a data size of said contents stored in said cache memory means; and when said size of said free space of said content storage means is equal to, or greater than, said data size of said contents stored in said cache memory means, said processor farther operable to write said contents processed or executed by said processor in said content storage means after reading said contents from said cache memory means."

Wong discloses the concept of "said processor is further operable to determine whether a size of a free space of said content storage means is equal to, or greater than, a data size of said contents stored in said cache memory means; and when said size of said free space of said content storage means is equal to, or greater than, said data size of said contents stored in said cache memory means, said processor farther operable to write said contents processed or executed by said processor in said content storage means after reading said contents from said cache memory means" as **[a process for writing an object to main memory by a cache controller wherein "cache controller 44 first determines whether the object to be written can fit in the buffer 62" (Columns 5-6, paragraph 0060)] "if the object fits in the object buffer 62, the object is written to object buffer 62" (Columns 5-6, paragraph 0060)]**.

Suzaki (US 2004/0078636), Pawate et al. (US 5,678,021) and Wong et al. (US 2004/0111443) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the content trial system which first stores contents in a cache and then transfers these contents to a content storage as described by Suzaki and Pawate and determine if there is

enough space in a content storage before transferring data to this content storage as taught by Wong.

The motivation for doing so would have been because Wong teaches that determining whether there is enough free space in memory before transferring data **["increases caching performance of persistent memory" (Column 1, paragraph 0003) and prevents system crashes as when there is not enough space in memory, the system prevents writing new objects to memory]**.

Therefore, it would have been obvious to combine Wong et al. (US 2004/0111443) with Suzaki (US 2004/0078636) and Pawate et al. (US 5,678,021) for the benefit of creating a content trial system to obtain the invention as specified in claim 8.

14. **Claims 9-10, 16 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzaki (US 2004/0078636) in view of Pawate et al. (US 5,678,021) and Wong et al. (US 2004/0111443) as applied to claims 8 above, and further in view of Spencer et al. (US 2003/0014496).

15. As per **claims 9 and 10** (New) A communication device according to Claim 8, wherein: "when said size of said free space of said content storage means is smaller than said data size of said contents stored in said cache memory means, said processor is further operable to" delete data as **["cache controller 44 purges entries from persistent memory 50 that are older than a particular age, and moves entries buffered in main memory 48 having dates greater than a particular age to persistent memory 50" and explains that "purging entries from persistent memory 50 frees up disk space, and moving entries from main memory 48 frees up buffer space" (Column 5, paragraph 0059)]**but does not disclose expressly "prompt a user

to delete one or more other contents stored in said content storage means; and when, in response to said prompt, a command is received via said operation input means to delete said one or more other contents stored in said content storage means, said processor is further operable to determine if, after deletion of said one or more other contents, said free space of said content storage means will be equal to, or greater than, said data size of said contents, said processor further operable to provide indication thereof to a user."

Spencer discloses the concept of "prompt a user to delete one or more other contents stored in said content storage means; and when, in response to said prompt, a command is received via said operation input means to delete said one or more other contents stored in said content storage means, said processor is further operable to determine if, after deletion of said one or more other contents, said free space of said content storage means will be equal to, or greater than, said data size of said contents, said processor further operable to provide indication thereof to a user." (***Pages 9-10, paragraph 0048 of Applicant's specification identifies this means as "CPU 400"***) as [**a device which downloads files through a computer network (Column 3, paragraph 0027) wherein "download manager 120;" (Figure 1) completes "the instructions for remote management can include instructions to add specific media content to existing media content on the digital playback device, or instructions to remove specific media content from the digital media playback device. The instructions to remove specific media content can be generated in response to a request form a user or be automatically generated" (Column 2, paragraph 0015) and provides and example in which when there is not enough space to download a file, the user is asked to delete on or more files residing on**

the device and the user is able to submit a command to delete selected files (Columns 10-11, paragraph 0084)].

Suzaki (US 2004/0078636), Pawate et al. (US 5,678,021), Wong et al. (US 2004/0111443) and Spencer et al. (US 2003/0014496) are analogous art because they are from the same field of endeavor of computer memory management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the content trial system which first stores contents in a cache and then transfers these contents to a content storage as described by Suzaki and Pawate and determine if there is enough space in a content storage before transferring data to this content storage as taught by Wong, and further prompt a user to delete contents of a storage device when there is not enough space to store new data as taught by Spencer.

The motivation for doing so would have been because Spencer teaches that a user prompted to delete contents of a storage device when there is not enough space to store new data **[in order to free space when new files must be downloaded to a storage device (Columns 10-11, paragraph 0084)]**.

Therefore, it would have been obvious to combine Spencer et al. (US 2003/0014496), Pawate et al. (US 5,678,021), Suzaki (US 2004/0078636) and Wong et al. (US 2004/0111443) for the benefit of creating a content trial system to obtain the invention as specified in claims 9-10.

16. As per **claim 16** (New) the combination of Suzaki and Pawate discloses the communication device of Claim 15, **[See rejection to claim 15 above]** wherein "the processor is operable to exit and automatically delete the temporarily stored content in response to receipt of

a user command to cease execution or processing of the temporarily stored content" **[The rationale in the rejection of claim 9 is herein incorporated]**.

17. As per **claim 18** (New) the combination of Suzaki and Pawate discloses the communication device of Claim 15, **[See rejection to claim 15 above]** wherein "the first storage area is a cache area of the memory, and the processor is further operable to delete data from the second storage area only in response to receipt of a user command to delete from the second storage area" **[The rationale in the rejection to claim 9 is herein incorporated]**.

III. RELEVANT ART CITED BY THE EXAMINER

18. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

19. The following reference teaches using cache memory for execution of applications.

U.S. PATENT NUMBER

US 6,931,488

IV. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

20. Applicant's arguments filed August 2, 2006 have been fully considered and are not persuasive.

21. As required by **M.P.E.P. § 707.07(f)**, a response to these arguments appears below.

V. ARGUMENTS CONCERNING PRIOR ART REJECTIONS

1st POINT OF ARGUMENT:

22. Applicant's remark that Suzaki does not disclose "cache memory means, to process or execute said contents automatically, absent receipt of a command initiated by a user" are moot in view of new grounds of rejection.

2nd POINT OF ARGUMENT:

23. Regarding Applicant's remark that Suzaki does not disclose "said processor, to read said contents from said cache memory means, and to write said contents in said content storage means," it is the Examiner's position that Suzaki discloses this limitation as [**"the MPU 72 and write-back switch 73 are controlled by OS kernel 75. The OS kernel 75 operates in accordance with requests from program 77 and trial settings 76" (Page 3, Paragraph 0038)**], therefore, Suzaki reading data from cache memory and writing this data to permanent storage as data is written back from cache memory to permanent storage.

24. All arguments by the applicant are believed to be covered in the body of the office action or in the above remarks and thus, this action constitutes a complete response to the issues raised in the remarks dated August 2, 2006.

VI. CLOSING COMMENTS

Conclusion

25. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing data of this action. In the event a first reply is filed within **two months** of the mailing date of this final action and the advisory action is not mailed until after the end of the **three-month** shortened statutory period, then the shortened statutory period will expire on the data the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing data of the advisory action. In no event, however, will the statutory period for reply expire later than **six months** from the mailing date of the final action.

VII. STATUS OF CLAIMS IN THE APPLICATION

26. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

27. Per the instant office action, **claims 6-24** have received a second action on the merits and are subject of a final rejection.

a(2) CLAIMS NO LONGER IN THE APPLICATION

28. Claims 1-5 were cancelled by the amendment dated August 2, 2006.

29. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VIII. DIRECTION OF ALL FUTURE REMARKS

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

31. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

32. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 13, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100